

CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A non-volatile memory cell comprising:
 - a semiconductor body region;
 - a first source/drain region located in the semiconductor body region and coupled to a first contact element;
 - a second source/drain region located in the semiconductor body region and coupled to a second contact element;
 - a gate electrode having a central portion located over a channel region located in the semiconductor body region between the first and second source/drain regions, a first end portion located on a first side of the central portion, and a second end portion located on a second side of the central portion;
 - a third contact element coupled to the first end portion of the gate electrode;
 - a fourth contact element coupled to the second end portion of the gate electrode; and
 - a fifth contact element coupled to the semiconductor body region;wherein the third and fourth contact elements allow for independent control of the first and second end portions of the gate electrode; and wherein the gate electrode exhibits agglomeration.
2. (Original) The non-volatile memory cell of Claim 1, wherein the gate electrode comprises a layer of polycrystalline silicon and a layer of metal silicide.

3. (Original) The non-volatile memory cell of Claim 2, wherein the layer of metal silicide comprises at least one of titanium silicide, cobalt silicide and nickel silicide.
4. (Original) The non-volatile memory cell of Claim 2, wherein the layer of metal silicide exhibits agglomeration.
5. (Original) The non-volatile memory cell of Claim 2, wherein first and second end portions of the gate electrode are wider than the central portion of the gate electrode.
6. (Original) The non-volatile memory cell of Claim 1, wherein the first and second source/drain regions have a p-type conductivity.
7. (Original) The non-volatile memory cell of Claim 6, wherein the semiconductor body region comprises an n-type well region.
8. (Original) The non-volatile memory cell of Claim 1, further comprising a gate dielectric layer located between the channel region and the gate electrode.
9. (Original) The non-volatile memory cell of Claim 1, wherein during programming, the third contact element is coupled to receive a first control voltage, and the fourth contact element is coupled to receive a second control voltage, which is less than the first control voltage.
10. (Original) The non-volatile memory cell of Claim 9, wherein during programming, the fifth contact element is coupled to receive a third control voltage, which is greater than the second control voltage.

11. (Original) The non-volatile memory cell of Claim 9, wherein the first and second control voltages are less than or equal to a normal operating voltage of a CMOS process.

12. (Original) The non-volatile memory cell of Claim 1, further comprising current sense circuitry for detecting a read current in the first source/drain region.

13. (Original) The non-volatile memory cell of Claim 1, wherein the non-volatile memory cell is fabricated using a standard CMOS process.

14. (Original) The non-volatile memory cell of Claim 1, wherein the non-volatile memory cell is part of a programmable read-only memory.

15. (Original) The non-volatile memory cell of Claim 1, wherein the non-volatile memory cell is part of a programmable logic device.

16. (Original) The non-volatile memory cell of Claim 1, wherein the non-volatile memory cell stores a portion of an encryption key.

17. (Original) The non-volatile memory cell of Claim 1, wherein the non-volatile memory cell selectively enables or disables a portion of a circuit coupled to the non-volatile memory cell.

18 – 26. (Canceled)

27. (Currently Amended) A system for enabling a transistor to be operated as a non-volatile memory cell, the system comprising:

means for applying a first program control voltage to a first end of a gate electrode of the transistor; and

means for applying a second program control voltage to a second end of the gate electrode of the transistor, wherein the first and second program control voltages cause a current to flow through the gate electrode of the transistor, thereby changing a threshold voltage of the transistor and causing agglomeration in the gate electrode of the transistor.

28. (Original) The system of Claim 27, wherein the first program control voltage is a positive supply voltage, and the second program control voltage is a ground supply voltage.

29. (Original) The system of Claim 27, further comprising means for applying a third program control voltage to a body region of the transistor, wherein the third program control voltage, combined with the first and second program control voltages, introduces a negative bias to the transistor.

30. (Original) The system of Claim 27, further comprising:

means for applying a first read control voltage to the first and second ends of the gate electrode, and to a first source/drain region of the transistor; and

means for applying a second read control voltage to the body of the transistor and a second source/drain region of the transistor.